Q.P. Code: 16EC408 **R16**

Reg. No: | | | | | | | | | | |

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY:: PUTTUR

(AUTONOMOUS)

B.Tech II Year II Semester Supplementary Examinations Dec 2019

COMPUTER ORGANIZAION & ARCHITECTURE

(ELECTRONICS AND COMMUNICATION ENGINEERING)

Time: 3 hours Max. Marks: 60

(Answer all Five Units **5 x 12 = 60** Marks)

UNIT-I

1	a	Sketch the internal organization of CPU out with its functionalities and block diagram.	**8M**
	b	Write about hierarchy of buses, bus signals and its functionalities.	**4M**
		OR	
2	a	List out the general aspects of ROM, RAM and I/O interfacing modules.	**4M**
	b	Design a relatively simple computer which incorporates 8K RAM, 8K ROM, I/O interfacing modules along with processor.	**8M**

UNIT-II

3	a	Implement hardware for multiplying two fixed- point binary numbers in signed-magnitude representation along with its flowchart.	**3M**
	b	Explain in detail about booth multiplication algorithm with an example.	**9M**
		OR	
4	a	What is the use of program control instructions? Mention its typical instructions.	**6M**
	b	Describe the importance of BCD in digital system design.	**6M**

UNIT-III

5	a	Design a 4-bit ALU which performs arithmetic, Logical and shift operations.	**5M**
	b	Explain about address sequencing in control memory with neat diagrams.	**7M**
		OR	
6	a	Implement a 4-bit combinational circuit shifter using Multiplexer.	**7M**
	b	Illustrate the phases involved in decoding of micro operation fields with necessary diagrams.	**5M**

UNIT-IV

7	a	Explain Virtual address Mapping using Pages with necessary examples.	**7M**
	b	Elaborate how DMA bypasses CPU and speeds up the memory operation.	**5M**
		OR	
8	a	What is Locality of Reference and explain about Cache memory in detail.	**5M**
	b	Discuss the Memory Hierarchy in computer system with regard to Speed, Size and Cost.	**7M**

UNIT-V

9	a	Illustrate the behavior of a pipeline using space-time diagram.	**8M**
	b	Justify how parallel processing improves the performance of multiprocessing environment	**4M**
		OR	
10	a	With examples, Explain four segment CPU pipeline and Timing of instruction pipeline.	**6M**
	b	Write about Time shared common bus and multiport memory.	**6M**

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